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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,254	12/31/2003	Kazuhide Abe	OKI 394	6980

23995 7590 07/29/2005

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EXAMINER	
COLEMAN, WILLIAM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/748,254	ABE, KAZUHIDE	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-8 have been considered but are moot in view of the new ground(s) of rejection.

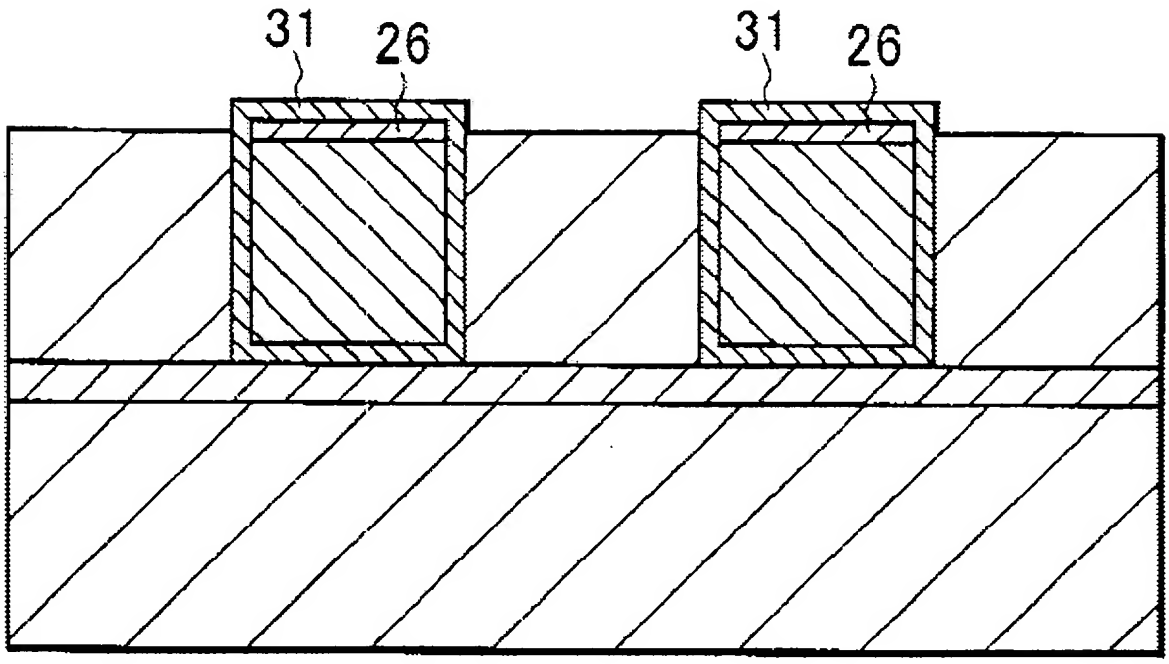
Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Komai et al., U.S. Patent 6,479,384 B2

Please see **FIGS. 1A-3B**.



3. Komai teaches the semiconductor manufacturing process as claimed.

4. Pertaining to claim 1, Komai teaches a method of manufacturing a semiconductor device, comprising the steps of:

embedding a copper wiring layer into a plug provided on a semiconductor substrate and a compound of copper into the copper wiring layer from thereabove respectively;

forming a reactive layer and a barrier metal layer interdiffused with the copper wiring layer on the compound of copper; and

interdiffusing the copper compound and the reactive layer by heat treatment to thereby form an alloy layer of copper between the copper wiring layer and the barrier metal layer (Komai uses the term catalytic which functions to the equivalent of interdiffused).

5. Pertaining to claim 2, Komai teaches the method according to claim 1, wherein the compound of copper is obtained by processing the copper wiring layer according to a method selected out of nitriding, oxidizing, boronizing, sulphidizing or phosphidizing (column 4, lines 49).

6. Pertaining to claim 3, Komai teaches the method according to claim 1, wherein the reactive layer is at least one kind of material selected from Ti, B, S, Sn, Ga, Ge, Hf, In, Mg, Ni, Nb, Pd, P, Sc, Se, Si, Zn, and Ag (column 4, line 46).

7. Pertaining to claim 4, Komai teaches the method according to claim 1, wherein. a barrier metal for the barrier metal layer is a material selected from CoSn, CoZ, CoW, Ti, TiN-, Ta, TaN, W, and WN.

8. Pertaining to claim 5, Komai teaches a method of manufacturing a semiconductor device, comprising the steps of: embedding a copper wiring layer into a plug provided on a semiconductor substrate and a compound of copper into the copper wiring layer from thereabove respectively;, forming a barrier metal layer containing a substance interdiffused with the copper wiring layer on the compound of copper; and allowing the compound of copper and the barrier metal layer to react by heat treatment to thereby form an alloy layer of copper and a barrier metal layer on the copper wiring layer.

9. Pertaining to claim 6, Komai teaches the method according to claim 5, wherein the compound of copper is obtained by processing the copper wiring layer according to a method selected out of nitriding, oxidizing, boronizing, sulphidizing or phosphidizing.

10. Pertaining to claim 7, Komai teaches the method according to claim 5, wherein the substance reacted with the copper is at least one kind of material selected from Ti, B, S, Sn, Ga, Ge, Hf, In, Mg, Ni, Nb,, Pd, P, Sc, Se, Si, Zn, and Ag.

11. Pertaining to claim 8, Komai teaches the method according to claim 5, wherein a barrier metal for the barrier metal layer is a material selected from Co, Sn, CoZ, CoW, Ti, TiN, Ta, TaN, W, and WN.

12. Pertaining to claim 9, Komai teaches the method according to claim 1, wherein the copper wiring layer is buried and the compound of copper is formed on an exposed surface of the copper wiring layer.

13. Pertaining to claim 10, Komai teaches the method according to claim 9, wherein the compound of copper is formed at a surface of the semiconductor substrate.

14. Pertaining to claim 11, Komai teaches the method according to claim 5, wherein the copper wiring layer is buried and the compound of copper is formed on an exposed surface of the copper wiring layer.

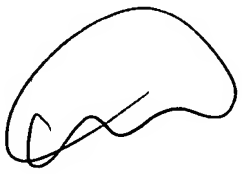
15. Pertaining to claim 12, the method according to claim 11, wherein the compound of copper is formed at a surface of the semiconductor substrate.

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

17. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

18. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



W. David Coleman
Primary Examiner
Art Unit 2823

WDC